



PIC16F506

PIC16F506 Rev. B1 Silicon Errata and Data Sheet Clarification

The Rev. B1 PIC16F506 family devices that you have received conform functionally to the current Device Data Sheet (DS41268D), except for the anomalies described in this document.

The silicon/specification issues discussed in the following pages are for silicon revision B1. If, however, questions do arise concerning the silicon revision received in a particular factory shipment, please contact your local Microchip sales office for assistance.

Silicon Errata

None.

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41268D):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Analog-to-Digital Converter (ADC)

The A/D Converter does not meet the design target. The specifications listed below in Table 1 supersede those of Table 13-3 in DS41268D. Also, the four graphs in Figure 1, Figure 2, Figure 3 and Figure 4 following Table 1 below show how the converter performs, when tested at a 7-bit level of resolution, in response to temperature changes at VDD levels of 2.0V and 5.5V.

TABLE 1: A/D CONVERTER CHARACTERISTICS AT 8 BITS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A03	EIL	Integral Error	—	—	±2	LSb	VDD = 5.0V 25°C
A04	EDL	Differential Error	—	—	-1 ≤ EDL ≤ 2	LSb	VDD = 5.0V 25°C
A06	E _{OFF}	Offset Error	—	—	±2	LSb	VDD = 5.0V 25°C
A07	E _{GN}	Gain Error	—	—	±2	LSb	VDD = 5.0V 25°C
A25	V _{AIN}	Analog Input Voltage	V _{SS} V _{SS}	— —	V _{DD} .9 V_{DD}	V V	T > 85°C and Fosc > 10 MHz only

* These parameters are characterized but not tested.

† Data in the “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only are not tested.

Work around

None.

FIGURE 1: TYPICAL DNL AT 2.0V (OPERATION AT 7-BIT LEVEL)

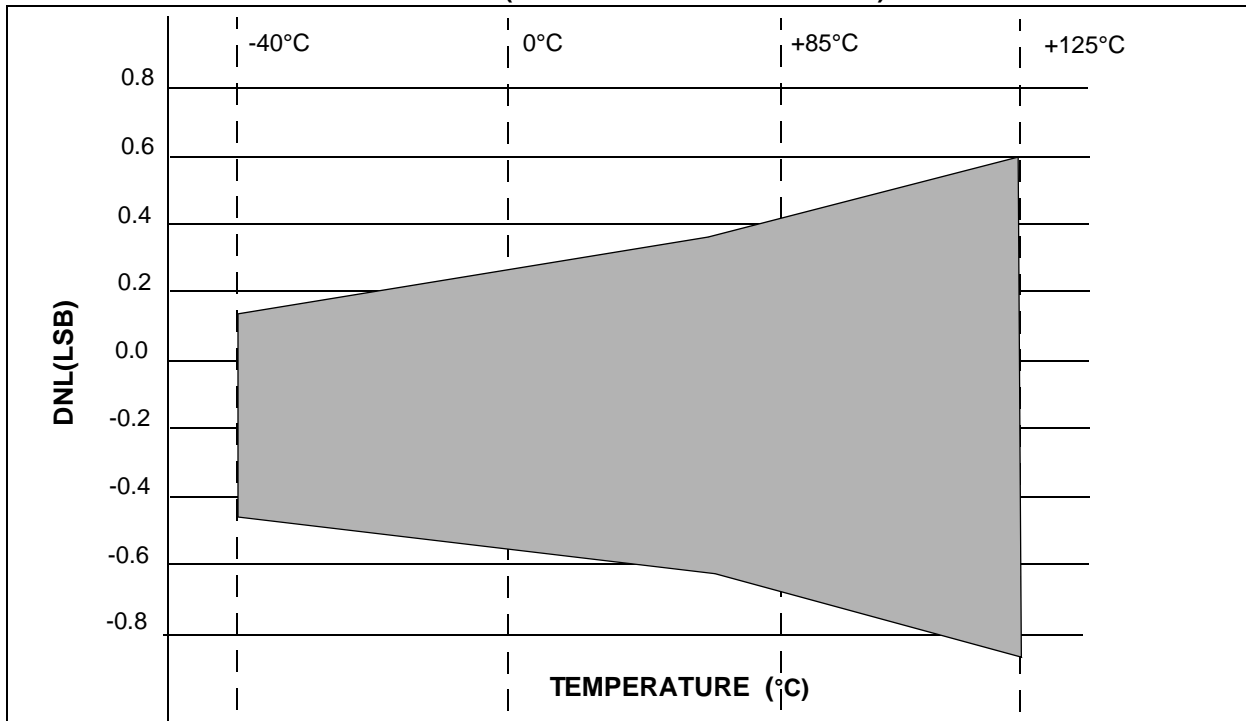


FIGURE 2: TYPICAL INL AT 2.0V (OPERATION AT 7-BIT LEVEL)

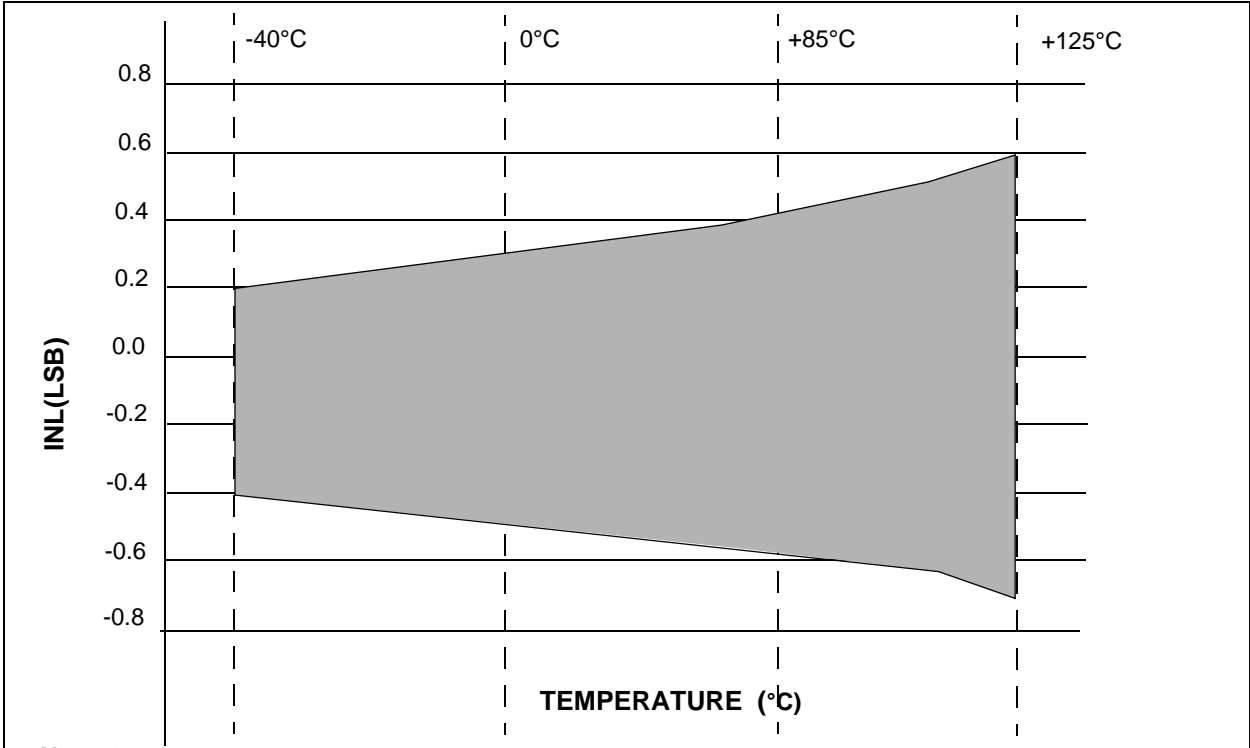
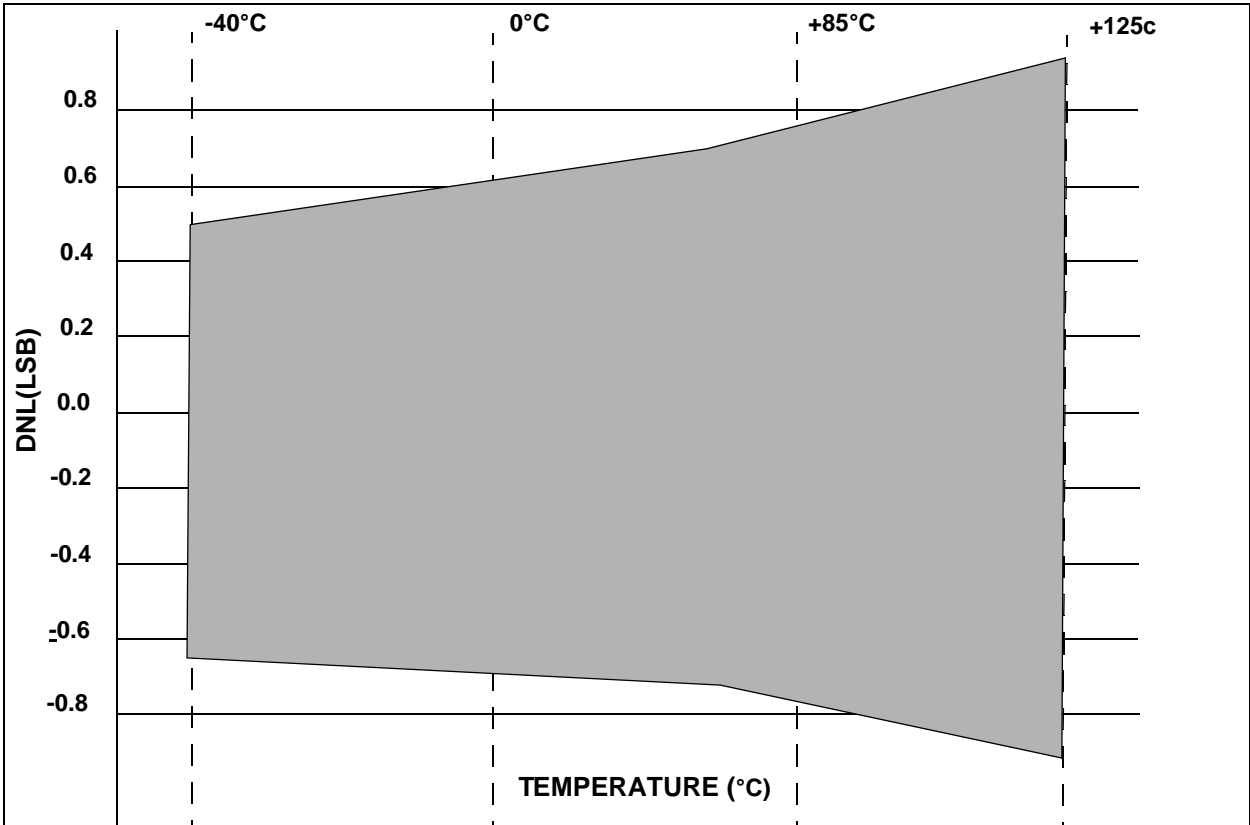
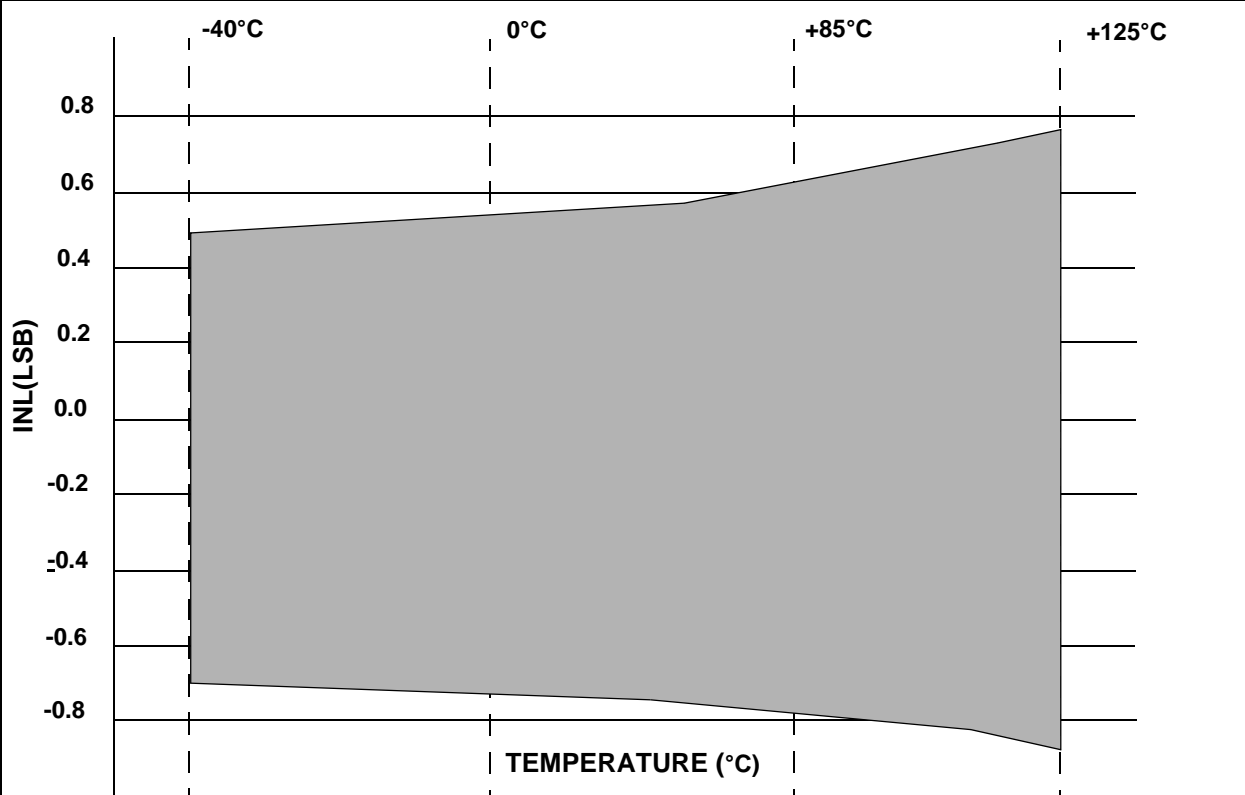


FIGURE 3: TYPICAL DNL AT 5.5V (OPERATION AT 7-BIT LEVEL)



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FIGURE 4: TYPICAL INL AT 5.5V (OPERATION AT 7-BIT LEVEL)



2. Module: Comparator Voltage Reference

Table 13-2 in data sheet DS41268D should read as follows:

TABLE 13-2: COMPARATOR VOLTAGE REFERENCE (VREF) SPECIFICATIONS

Sym	Characteristics	Min	Typ	Max	Units	Comments
CVRES	Resolution	—	VDD/24*	—	LSb	Low Range (VRR = 1)
		—	VDD/32	—	LSb	High Range (VRR = 0)
	Absolute Accuracy ⁽²⁾	—	—	±1/2*	LSb	Low Range (VRR = 1)
		—	—	±1/2*	LSb	High Range (VRR = 0)
Unit Resistor Value (R)	—	2K*	—	Ω		
	Settling Time ⁽¹⁾	—	—	10*	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

2: Do not use reference externally when VDD < 2.7V. Under this condition, reference should only be used as a comparator input with all input common mode voltage range limitations observed.

Work around

None.

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3. Module: Analog-to-Digital Converter (ADC)

The Reset value for the ADCON0 register is updated for Resets other than Power-on Reset. Changes to the table affected are listed in Table 10-4 below and are identified in bold and italic text.

TABLE 10-4: RESET CONDITIONS FOR REGISTERS – PIC16F506

Register	Address	Power-on Reset	$\overline{\text{MCLR}}$ Reset, WDT Time-out, Wake-up on Pin Change, Wake-up on Comparator Change
W	—	qqqq qqqu ⁽¹⁾	qqqq qqqu ⁽¹⁾
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	10uq quuu ⁽²⁾
FSR	04h	100x xxxx	10uu uuuu
OSCCAL	05h	1111 111-	uuuu uu-
PORTB	06h	--xx xxxx	--uu uuuu
PORTC	07h	--xx xxxx	--uu uuuu
CM1CON0	08h	1111 1111	uuuu uuuu
ADCON0	09h	1111 1100	1111 1100
ADRES	0Ah	xxxx xxxx	uuuu uuuu
CM2CON0	0Bh	1111 1111	uuuu uuuu
VRCON	0Ch	0011 1111	uuuu uuuu
OPTION	—	1111 1111	1111 1111
TRISB	—	--11 1111	--11 1111
TRISC	—	--11 1111	--11 1111

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Note 1: Bits <7:1> of W register contain oscillator calibration values due to MOV LW XX instruction at top of memory.

2: See Table 10-5 for Reset value for specific conditions.

Work around

None.

4. Module: Electrical Characteristics

The min. and max. values in Table 13-1 for Internal Voltage Reference (VIVRF) have been revised. Changes to the table are listed below and identified in bold and italic text.

TABLE 13-1: COMPARATOR SPECIFICATIONS

Sym	Characteristics	Min	Typ	Max	Units	Comments
VOS	Input Offset Voltage	—	±3	±10	mV	(VDD - 1.5V)/2
VCM	Input Common Mode Voltage	0	—	VDD - 1.5	V	
CMRR	Common Mode Rejection Ratio	+55*	—	—	dB	
TRT	Response Time ⁽¹⁾	—	150	400*	ns	Internal
VIVRF	Internal Voltage Reference	0.500	0.6	0.700	V	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD - 1.5)/2, while the other input transitions from VSS to VDD - 1.5V.

Work around

None.

5. Module: Electrical Characteristics

The typ. value at 5V VDD and the max. values at 2V and 5V VDD have been revised as shown in Table 2 below.

TABLE 2: ICMP

DC Characteristics			Standard Operating Conditions (unless otherwise specified)				Conditions
Param No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	
D023	ICMP	Comparator Current⁽²⁾	—	15	26	μA	VDD = 2.0V (per comparator)
			—	60	76	μA	VDD = 5.0V (per comparator)

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: For standby current measurements, the conditions are the same as IDD, except that the device is in Sleep mode. If a module current is listed, the current is for that specific module enabled and the device in Sleep.

Work around

None.

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6. Module: Electrical Characteristics

The max. values at 2V and 5V V_{DD} for LP Oscillator I_{DD} at 125°C have been revised as shown in Table 3 below.

TABLE 3: LP OSCILLATOR 125°C I_{DD}

DC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ T _A ≤ +125°C (extended)				
Param No.	Sym.	Characteristics	Min.	Typ ⁽¹⁾	Max.	Units	Conditions
D010	I _{DD}	Supply Current ^(2,3)	—	11	24	μA	FOSC = 32 kHz, V _{DD} = 2.0V
			—	38	110	μA	FOSC = 32 kHz, V _{DD} = 5.0V

- Note 1:** Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.
- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.
- 3:** The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{SS}, T0CKI = V_{DD},
MCLR = V_{DD}; WDT disabled unless noted otherwise.

Work around

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (01/2007)

First revision of this document.

Rev B Document (08/2009)

Updated document to new format; Updated the title of the errata.

Data Sheet Clarifications: Added Module 1, from the old version of this errata, to Data Sheet Clarifications; Added Module 2; Removed Table 9-2; Added Modules 3, 4, 5 and 6; Other minor edits.

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NOTES:

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